Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of testing [[a]] semiconductor storage devices of common type [[device]], comprising the steps of:

setting a plurality of test patterns in a tester for testing the semiconductor storage devices;

applying different test patterns to the respective semiconductor storage devices connected to said tester; and

determining whether or not results of the tested semiconductor storage devices fall within a predetermined tolerance.

2. (Currently Amended) The method of testing [[a]] semiconductor storage devices of common type [[device]] according to claim 1, wherein the number of defective bit lines of said tested semiconductor storage device having exceeded a tolerance is compared with the number of redundant lines on the basis of a test result output, thereby determining semiconductor storage devices which can be restored through use of redundant lines.

3. (Currently Amended) The method of testing [[a]] semiconductor storage devices of common type [[device]] according to claim 1, wherein the number of defective column lines of said tested semiconductor storage device having exceeded a tolerance is compared with the

number of redundant lines on the basis of a test result output, thereby determining semiconductor storage devices which can be restored through use of redundant lines.

4. (Currently Amended) The method of testing [[a]] semiconductor storage devices of common type [[device]] according to claim 1, wherein a test is performed several times while a test pattern is changed.

5. (Currently Amended) The method of testing [[a]] semiconductor storage devices of common type [[device]] according to claim 1, wherein, when said tested semiconductor storage devices are non-volatile, the devices are subjected to writing and erasure tests.

6. (Currently Amended) The method of testing [[a]] semiconductor storage devices of common type [[device]] according to claim 1, wherein a test pattern is made by combination of a voltage, a time, and a signal.